Claims

What is claimed is:

1. A method for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs comprising the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library;

for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET to provide a hybrid alternate voltage threshold (AVT) circuit; and

saving each said AVT circuit in an alternate circuit library.

2. A method for implementing enhanced performance and reduced leakage current as recited in claim 1 wherein the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) over each said SVT PFET.

3. A method for implementing enhanced performance and reduced leakage current as recited in claim 2 wherein the step of adding a low voltage threshold (LVT) over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFETs to said LTV PFET.

4. An alternate voltage threshold (AVT) circuit library comprising:

a plurality of hybrid AVT circuits, each said hybrid AVT circuit including

each P-channel field effect transistor (PFET) having a low voltage threshold (LVT); and

each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT).

5. An alternate voltage threshold (AVT) circuit library as recited in claim 4 wherein said hybrid AVT circuits include a corresponding standard voltage threshold (SVT) having a low voltage threshold (LVT) added over each said SVT PFET to convert each said SVT PFET to said LVT PFET.

6. An alternate voltage threshold (AVT) circuit library as recited in claim 4 wherein each said LVT PFET are provided in an Nwell Region isolated from each said NFET in each said hybrid AVT circuit.

7. A computer program product for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library;

for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET to provide a hybrid alternate voltage threshold (AVT) circuit; and

saving each said AVT circuit in an alternate circuit library.

8. A computer program product as recited in claim 7 wherein the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) over each said SVT PFET.

9. A computer program product as recited in claim 8 wherein the step of adding a low voltage threshold (LVT) over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET.